This listing of the claims will replace all prior versions, and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently amended) A method of forming a substantially planar diamond coated silicon wafer comprising:

forming a diamond coated silicon wafer comprising forming a diamond layer on a silicon substrate that induces a compressive stress in the silicon substrate, wherein the diamond layer is formed at a temperature below a CTE crossover temperature; and

tuning the planarity of the diamond coated silicon wafer by roughening a first surface of the diamond coated silicon wafer.

2. (Original) The method of claim 1 wherein roughening the first surface of the diamond coated silicon wafer induces a tensile stress that cancels the compressive stress in the silicon substrate.

3. (Original) The method of claim 1 wherein tuning the planarity of the diamond coated silicon wafer comprises decreasing the magnitude of a first surface first deflection and a second surface first deflection in the diamond coated silicon wafer.

4. (Canceled)

5. (Currently amended) The method of ~~claim 4~~ claim 1 wherein ~~forming~~ the diamond layer is formed at a temperature below a CTE crossover temperature comprises

forming the diamond layer from about 600 degrees Celsius to about 1100 degrees Celsius.

6. (Currently amended) The method of ~~claim 5~~ claim 1 wherein forming the diamond layer comprises forming the diamond layer by PECVD.

7. (Original) The method of claim 6 wherein forming the diamond layer by PECVD comprises applying a temperature gradient across the silicon substrate that is within about 50 degrees of the CTE crossover temperature.

8. (Original) The method of claim 1 wherein roughening the first surface of the diamond coated silicon wafer comprises grinding.

9. (Original) The method of claim 1 wherein roughening the first surface of the diamond coated silicon wafer comprises introducing defects in the first surface of the diamond coated silicon wafer.

10. (Original) A method of forming a substantially planar diamond coated silicon wafer comprising:

forming a diamond coated silicon wafer comprising forming a diamond layer on a silicon substrate that induces a compressive stress in the silicon substrate; and

tuning the planarity of the diamond coated silicon wafer by forming a first polysilicon layer on a first surface of the diamond coated silicon wafer.

11. (Original) The method of claim 10 wherein forming the first polysilicon layer on the first surface of the diamond coated silicon wafer induces a tensile stress that cancels the compressive stress in the silicon substrate.

12. (Original) The method of claim 10 wherein tuning the planarity of the diamond coated silicon wafer comprises decreasing the magnitude of a first surface first deflection and a second surface first deflection in the diamond coated silicon wafer.

13. (Original) The method of claim 10 wherein tuning the planarity of the diamond coated silicon wafer further comprises forming a second polysilicon layer on a second surface of the diamond coated silicon wafer.

14. (Original) The method of claim 13 wherein forming the first polysilicon layer and the second polysilicon layer comprises forming the first polysilicon layer and the second polysilicon layer by PECVD.

15. (Original) A method of forming a strained silicon device comprising:

providing a flatness tuned diamond coated silicon wafer wherein a first surface of the flatness-tuned diamond coated silicon wafer comprises defects;

forming a first polysilicon layer on a first surface of the flatness-tuned diamond coated silicon wafer and a second polysilicon layer on a second surface of the flatness-tuned diamond coated silicon wafer,

bonding a silicon device layer to the second polysilicon layer;

forming a plurality of circuit components on the silicon device layer; and

substantially removing the defects from the first surface of the flatness-tuned diamond coated silicon wafer to induce a tensile strain in the silicon device layer.

16. (Original) The method of claim 15 wherein substantially removing the defects from the first surface of the flatness-tuned diamond coated silicon wafer comprises;

removing the first polysilicon layer; and

substantially removing the defects from the first surface of the flatness-tuned diamond coated silicon wafer.

17. (Original) The method of claim 15 wherein bonding the silicon device layer comprises bonding the silicon device layer to the second polysilicon layer and polishing the bonded silicon device layer to the desired thickness.

18. (Original) The method of claim 15 wherein bonding the silicon device layer comprises bonding an oxidized silicon device layer to the second polysilicon layer, wherein a SOI structure is formed.

19. (Original) The method of claim 15 wherein bonding the silicon device layer comprises bonding the silicon device layer to the second polysilicon layer by layer transfer.

20. (Original) The method of claim 15 wherein forming the flatness tuned diamond coated silicon wafer comprises forming a substantially zero stress flatness-tuned diamond coated silicon wafer.

21. (Original) A method of forming a strained silicon device comprising:

providing a flatness tuned diamond coated silicon wafer comprising a first polysilicon layer disposed on a first surface of the flatness tuned diamond coated silicon wafer and a second polysilicon layer on a second surface of the flatness tuned diamond coated silicon wafer;

bonding a silicon device layer to the second polysilicon layer;

forming a plurality of circuit components on the silicon device layer; and

substantially removing the first polysilicon layer from the first surface of the flatness tuned diamond coated silicon wafer to induce a tensile strain in the silicon device layer.

22. (Original) The method of claim 21 wherein providing the flatness tuned diamond coated silicon wafer comprises providing a substantially zero stress flatness tuned diamond coated silicon wafer.

23. (Currently amended) A microelectronic structure, comprising:

a diamond layer on a silicon substrate; and

a strained silicon device layer on the diamond layer, wherein the strained silicon device layer comprises a tensile strain greater than about 1 percent.

24. (Canceled)

25. (Original) The structure of claim 23 wherein the strained silicon device layer comprises a plurality of circuit components.

26. (Original) The structure of claim 23 wherein the strained silicon device layer comprises a silicon on insulator (SOI) structure.

27. (Original) The structure of claim 23 wherein the diamond layer is between about 25 and 200 microns thick.